# Distinguished Lecture: 3D MIM Capacitor Embedded in TSV: Concept, Device Demonstration, Reliability and Applications

**Date:**
**29 July 2021**

**Time:**
**18:00 to 19:00**

**Location:**
**Zoom platform**

**Space is limited**

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## Synopsis

In this work, a novel integrated capacitor, called "3D MIM Capacitor Embedded in TSV" is proposed, designed, fabricated, and characterized for application in integrated circuits (ICs) with through-silicon vias (TSVs). A significant capacitance density enhancement can be achieved for this 3D embedded capacitor, because it leverages on the high aspect ratio structure of TSVs. Compared to conventional trench capacitor, this technology does not consume additional silicon area because it is embedded in the trenches of existing TSVs, instead of dedicated trenches. An ultrahigh capacitance density of 5,621.8 nF/mm2 was envisioned according to our model, which is ~13× of 440.0 nF/mm2 from a conventional trench capacitor with the same design parameters. A leakage current density as low as 1.61×10-7 A/cm2 at 4.3V and a breakdown voltage greater than 9.5 V were measured for a sample with a capacitance density of 3,776.6 nF/mm2. In addition, the reliability of the 3D MIM and potential new applications it enables are discussed.

## Speaker

Chuan Seng Tan, PhD
Nanyang Technological University, Singapore

Chuan Seng Tan is a Professor of Electronic Engineering at the School of Electrical and Electronic Engineering at Nanyang Technological University, Singapore. He received his PhD from MIT in 2006. Currently, he is working on process technology of three-dimensional integrated circuits (3-D ICs), as well as engineered substrate (Si/Ge/Sn) for group-IV photonics. He has numerous publications (journal and conference) and IPs on 3-D technology and engineered substrates. Nine of his inventions have since been licensed to a spin-off company. He co-edited/co-authored five books on 3D packaging technology.
He is a senior member of IEEE and a recipient of the Exceptional Technical Achievement Award from the IEEE Electronics Packaging Society (EPS) in 2019. Since June 2019, he is a Distinguished Lecturer with IEEE-EPS. He is a Fellow of the International Microelectronics Assembly and Packaging Society (IMAPS) since 2019 and a recipient of the William D. Ashman - John A. Wagnon Technical Achievement Award in 2020.
He was the Chair of the Interconnections Sub-Committee for ECTC'2021. He was the General Chair of the 2020 IEEE Electronics Packaging Technology Conference (EPTC-Virtual). In addition, he is an Associate Editor for the IEEE Transactions on Components, Packaging and Manufacturing Technology and was recognised with the Best Associate Editor Award in 2021.

**Co-organizer**

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